

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (previously presented): A common drive circuit for a display, the common drive circuit comprising:

a first voltage supply and a second voltage supply which respectively supply a high level voltage signal and a low level voltage signal to a common electrode;

at least one first transistor including either a drain or a source terminal connected to said first voltage supply;

at least one second transistor including either a drain or source terminal connected to said second voltage supply;

at least one signal line connected to each gate terminal of said first and second transistor;
and

at least one capacitance load connected to respective terminals of said first and said second transistors not connected to said first and second voltage supplies,

wherein a high level of a signal passing through the at least one signal line is higher than the high level voltage signal supplied by said first voltage supply and a low level of the signal passing through the signal line is lower than the low level voltage signal supplied by said second voltage supply.

2. (previously presented): The common drive circuit according to claim 1,

wherein at least said common drive circuit, a display portion and a gate driver circuit for controlling switching of pixels of each line in said display portion are mounted on a substrate, and

wherein said common drive circuit is disposed on a position opposite to said gate driver circuit and said display portion therebetween.

3. (previously presented): The common drive circuit according to claim 1, wherein said at least one first transistor comprises P-type transistor and said at least one second transistors comprises N-type transistor, and wherein said gate terminals of said first and second transistors are connected to common signal lines.

4. (previously presented): The common drive circuit according to claim 2, wherein P-type transistors and N-type transistors are connected in parallel to be said first transistor, and N-type transistors and P-type transistors are connected in parallel to be said second transistor,

wherein respective gates of said P-type transistors of said first transistor and said N-type transistor of said second transistors are connected to one said signal line, and respective gates of the N-type transistors of said first transistor and the P-type transistors of said second transistor are connected to an inversion signal line of one said signal line.

5. (previously presented): The common drive circuit according to claim 4,

wherein a high-level voltage of each signal of said signal line and said inversion signal line is a high-level line voltage of said gate driver and

wherein a low-level voltage of each signal of said signal line and said inversion signal line is a low-level line voltage of said gate driver.

6. (previously presented): The common drive circuit according to claim 2, wherein said first and second transistors are comprised of thin-film transistors.

7. (previously presented): The common drive circuit according to claim 2, wherein said display portion comprises a liquid crystal display.

8. (withdrawn): A voltage generating circuit for generating a providing voltage to a drive circuit comprising:

a first and a second variable resistances for adjusting said providing voltage;

a first operational amplifier outputting a high level of said providing voltage, and a non-inversion input thereof connected to a variable portion of said second variable resistance;

a second operational amplifier outputting a low level of said providing voltage, and a non-inversion input thereof connected to a variable portion of said second variable resistance;

a first resistance connecting a variable portion of said first variable resistances to an inversion input of said first operational amplifier;

a second resistance wherein one terminal of said second resistance connected to said inversion input of said first operational amplifier, and the other terminal of said second resistance connected to output of said first operational amplifier;

a third resistance connecting a constant voltage supply to an inversion input of said second operational amplifier;

a fourth resistance wherein one terminal of said fourth resistance connects to a inversion input of said second operational amplifier, and the other terminal of said fourth resistance connects to an output of said second operational amplifier;

wherein total resistance of said first variable resistance is a resistance value of one third or less of at least one of the total resistance of said second variable resistance and resistance of said first operational amplifier, said second operational amplifier, said first resistance, said second resistance, said third resistance, and said fourth resistance; and

wherein said first and second variable resistances adjust a low level of said providing voltage and a voltage difference between a high level and the low level of said providing voltage.

9. (withdrawn): The voltage generating circuit according to claim 8,

wherein said voltage generating circuit, a display portion, a drive circuit, a gate driver circuit for controlling switching of pixels of each line in said display portion are mounted on a substrate and

wherein said voltage generating circuit and said driving circuit are disposed opposite to said gate driver circuit and said display portion therebetween.

10. (withdrawn): A voltage generating circuit for generating a providing voltage to a drive circuit comprising:

a first and a second variable resistances for adjusting said providing voltage;

a first operational amplifier outputting a high level of said providing voltage, and a non-inversion input thereof connected to a variable portion of said second variable resistance;

a second operational amplifier outputting a low level of said providing voltage, and a non-inversion input thereof connected to a variable portion of said second variable resistance;

a first resistance connecting a variable portion of said first variable resistances to an inversion input of said first operational amplifier;

a second resistance wherein one terminal of said second resistance connected to said inversion input of said first operational amplifier, and the other terminal of said second resistance connected to output of said first operational amplifier;

a first capacitance, wherein one terminal of said first capacitance is connected to said output of said first operational amplifier, and the other terminal of said first capacitance connected to a constant voltage;

a third resistance connecting a constant voltage supply to an inversion input of said second operational amplifier;

a fourth resistance wherein one terminal of said fourth resistance connects to a inversion input of said second operational amplifier, and the other terminal of said fourth resistance connects to an output of said second operational amplifier;

a second capacitance, wherein one terminal of said second capacitance is connected to said output of said second operational amplifier, and the other terminal of said second capacitance connected to the constant voltage,

wherein total resistance of said first variable resistance is one third or less of at least one of the total resistance values of said second variable resistance and resistance of said first

operational amplifier, said second operational amplifier, said first resistance, said second resistance, said third resistance, and said fourth resistance .

11. (withdrawn): The voltage generating circuit according to claim 10,
wherein said voltage generating circuit, a display portion, said drive circuit, and a gate driver circuit for controlling switching of pixels of each line in a display portion are mounted on a substrate, and

wherein said voltage generating circuit and said driving circuit are disposed on a position opposite to said gate driver circuit and said display portion therebetween.

12. (withdrawn): The voltage generating circuit according to claim 9,
wherein at least one of said resistances and said capacitances are disposed outside said substrate, and are connected through an input pad of said display portion.

13. (withdrawn): The voltage generating circuit according to claim 11,
wherein at least one of said resistances and said capacitances are disposed outside said substrate, and are connected through an input pad of said display portion.

14. (withdrawn): The voltage generating circuit according to claim 9,
wherein said drive circuit comprises a drive circuit comprising; a first voltage supply, a second voltage supply for providing a voltage that is lower than a voltage of said first voltage supply, at least one first transistor including either a drain or a source terminal connected to said first voltage supply, at least one second transistor including either a drain or source terminal connected to said second voltage supply, at least one signal line connected to each gate

terminal of said first and second transistor, and at least one capacitance load connected to respective terminals of said first and said second transistors not connected to said first and second voltage supplies, wherein said signal line conveys signals having a high level that is substantially the same or higher than the voltage of said first voltage supply and having a low level that is substantially same or lower than the voltage of said second voltage supply.

15. (withdrawn): The voltage generating circuit according to claim 11,
wherein said drive circuit comprises a drive circuit comprising; a first voltage supply, a second voltage supply for providing a voltage that is lower than a voltage of said first voltage supply, at least one first transistor including either a drain or k' source terminal connected to said first voltage supply, at least one second transistor including either a drain or source terminal connected to said second voltage supply, at least one signal line connected to each gate terminal of said first and second transistor, and at least one capacitance load connected to respective terminals of said first and said second transistors not connected to said first and second voltage supplies, wherein said signal line conveys signals having a high level that is substantially the same or higher than the voltage of said first voltage supply and having a low level that is substantially the same or lower than the voltage of said second voltage supply.

16. (previously presented): A display comprising:
a substrate;
a display portion integrated on said substrate; and

a gate driver circuit which controls switching of pixels of each line in a display portion;
a common drive circuit for said display portion which simultaneously driving capacitance loads in said display portion,
wherein said common drive circuit is disposed on a position opposite to said gate driver circuit and said display portion therebetween.

17. (currently amended): The display according to claim 16, wherein said drive circuit comprises:

a first voltage supply and a second voltage supply which respectively supply a high level voltage signal and a low level voltage signal to a common electrode;

at least one first transistor including either a drain or a source terminal connected to said first voltage supply;

at least one second transistor including either a drain or source terminal connected to said second voltage supply;

at least one signal line connected to each gate terminal of said first and second transistor;
and

at least one capacitance load connected to respective terminals of said first and said second transistors that are not connected to said first and second voltage supplies,

wherein a high level of a signal passing through the at least one signal line is ~~the same or~~ higher than the high level voltage signal supplied by said first voltage supply and a low level of the signal passing through the signal line is ~~the same or~~ lower than the low level voltage signal supplied by said second voltage supply.

18. (original): The display unit according to claim 17,
wherein said at least first transistor comprises P-type transistors and said at least second transistor comprises N-type transistors, and
wherein said gate terminals of said first and second transistors are connected to common signal lines.

19. (original): The display unit according to claim 17,
wherein P-type transistors and N-type transistors are connected in parallel to be said first transistor, and N-type transistors and P-type transistors are connected in parallel to be said second transistor,
wherein respective gates of said P-type transistors of said first transistor and said N-type transistors of said second transistor are connected to one said signal line, and respective gates of the N-type transistors of said first transistor and the P-type transistors of said second transistor are connected to an inversion signal line of one said signal line.

20. (previously presented): The display unit according to claim 19,
wherein a high-level voltage of each signal of said signal line and said inversion signal line is a high-level line voltage of said gate driver, and
wherein a low-level voltage of each signal of said signal line and said inversion signal line is a low-level line voltage of said gate driver.

21. (original): The display unit according to claim 17, wherein all of said transistors are comprised of thin-film transistors.

22. (withdrawn): A display comprising:

- a substrate;
- a display portion integrated on said substrate;
- a gate driver circuit for controlling switching of pixels of each line in said display portion;
- a drive circuit for said display portion for simultaneously driving capacitive loads in said display portion; and
- a voltage generating circuit for generating a providing voltage to said drive circuit, wherein said voltage generating circuit disposed at a position opposite to said gate driver circuit and said display portion therebetween.

23. (withdrawn): The display unit according to claim 22,

wherein said voltage generating circuit comprises first and second variable resistances for adjusting said providing voltage, a first and a second variable resistances for adjusting said providing voltage, a first operational amplifier outputting a high level of said providing voltage, and a non-inversion input thereof connected to a variable portion of said second variable resistance, a second operational amplifier outputting a low level of said providing voltage, and a non-inversion input thereof connected to a variable portion of said second variable resistance, a first resistance connecting a variable portion of said first variable resistances to an inversion input of said first operational amplifier, a second resistance wherein one terminal of said second resistance connected to said inversion input of said first operational amplifier, and the other terminal of said second resistance connected to output of said first operational amplifier, a third resistance connecting a constant voltage supply to an inversion input of said second operational

amplifier, and a fourth resistance wherein one terminal of said fourth resistance connects to a inversion input of said second operational amplifier, and the other terminal of said fourth resistance connects to an output of said second operational amplifier,

wherein total resistance of said first variable resistance is a resistance value of one third or less of at least one of the total resistance of said second variable resistance and resistance of said first operational amplifier, said second operational amplifier, said first resistance, said second resistance, said third resistance, and said fourth resistance; and

wherein said first and second variable resistances adjust a low level of said providing voltage and a voltage difference between a high level and the low level of said providing voltage.

24. (withdrawn): The display unit according to claim 22,

wherein said voltage generating circuit comprises a first and a second variable resistances for adjusting said providing voltage;

a first operational amplifier outputting a high level of said providing voltage, and a non-inversion input thereof connected to a variable portion of said second variable resistance;

a second operational amplifier outputting a low level of said providing voltage, and a non-inversion input thereof connected to a variable portion of said second variable resistance;

a first resistance connecting a variable portion of said first variable resistances to an inversion input of said first operational amplifier;

a second resistance wherein one terminal of said second resistance connected to said inversion input of said first operational amplifier, and the other terminal thereof connected to output of said first operational amplifier;

a first capacitance connected to said output of said first operational amplifier, and the other terminal thereof connected to a constant voltage;

a third resistance connecting a constant voltage supply to an inversion input of said second operational amplifier;

a fourth resistance wherein one terminal thereof connects to a inversion input of said second operational amplifier, and the other terminal thereof connects to an output of said second operational amplifier;

a second capacitance wherein one terminal thereof connected to said output of said second operational amplifier, and the other terminal thereof connected to the constant voltage, wherein total resistance of said first variable resistance is one third or less of other resistance values.

25. (withdrawn): The display unit according to claim 23, wherein said drive circuit comprises a drive circuit comprising a first voltage supply, a second voltage supply for providing a voltage that is lower than a voltage of said first voltage supply, at least one first transistor including either a drain or a source terminal connected to said first voltage supply, at least one second transistor including either a drain or source terminal connected to said second voltage supply, at least one signal line connected to each gate terminal of said first and second transistor, and at least one capacitance load connected to respective terminals of said first and said second transistors not connected to said first and second voltage supplies, wherein said signal line conveys signals having a high level that is substantially the same or higher than the voltage of said first voltage supply and having a low level that is substantially the same or lower than the voltage of said second voltage supply.

26. (withdrawn): The display unit according to claim 24, wherein said drive circuit comprises a drive circuit comprising a first voltage supply,

a second voltage supply for providing a voltage that is lower than a voltage of said first voltage supply, at least one first transistor including either a drain or a source terminal connected to said first voltage supply, at least one second transistor including either a drain or source terminal connected to said second voltage supply, at least one signal line connected to each gate terminal of said first and second transistor, and at least one capacitance load connected to respective terminals of said first and said second transistors not connected to said first and second voltage supplies, wherein said signal line conveys signals having a high level that is substantially the same or higher than the voltage of said first voltage supply and having a low level that is substantially the same or lower than the voltage of said second voltage supply.

27-28. (canceled).

29. (previously presented): A common driver circuit according to claim 1, further comprising a level shift circuit connected to said one signal line directly or via a buffer circuit.

30. (previously presented): A common driver circuit according to claim 4, further comprising a level shift circuit connected to said at least one signal line and said inversion signal line directly or via a buffer circuit or an inverter circuit.

31. (previously presented): The display according to claim 17, further comprising a level shift circuit connected to said one signal line directly or via a buffer circuit or an inverter circuit.

32. (previously presented): The display according to claim 19, further comprising a level shift circuit connected to said at least one signal line and said inversion signal line directly or via a buffer circuit or an inverter circuit.